ABSTRACT OF THE DISCLOSURE

In order to achieve a redundant repair for a memory using a BIST, a semiconductor integrated circuit which can suppress an increase in circuit area for redundant repair and circuit area for scan test, and an test method thereof are provided. It comprises: a memory 104, which has a redundant line for repair in a Column direction; a test pattern generating section 101; a comparing section 102, which judges whether a faulty cell exists in the memory 104 or not, a first data storage section 105, which during an test of the memory 104, retrieves a signal inputted into the memory 104 from the test pattern generating section 101 and a pass/fail judgment signal for every bit from the comparing section 102, and during an test of a peripheral logic of the memory, is used for observing an input signal into the memory 104; a second data storage section 106, which shows a state of the presence or absence of a failure; and a repair judging section 107, wherein data of the first data storage section 105 is held by the second data storage section 106.